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Arild WEGO ) Group Art Unit: 2661
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Application No.: 10/000,038 ) Examiner: Unassigned
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Filed: December 4, 2001 )
)
For: ARRANGEMENT AND METHOD FOR TRANSMITTING DATA OVER A TDM BUS )



## CLAIM FOR CONVENTION PRIORITY

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The benefit of the filing date of the following prior foreign application in the following foreign country is hereby requested, and the right of priority provided in 35 U.S.C. § 119 is hereby claimed:

Norwegian Patent Application No. 20006185

Filed: December 5, 2000

In support of this claim, enclosed is a certified copy of said prior foreign application. Said prior foreign application was referred to in the oath or declaration. Acknowledgment of receipt of the certified copy is requested.

Respectfully submitted,

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Date: April 16, 2002

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# Bekreftelse på patentsøknad nr

*Certification of patent application no*

# 2000 6185

Det bekreftes herved at vedheftede dokument er nøyaktig utskrift/kopi av ovennevnte søknad, som opprinnelig inngitt 2000.12.05

*It is hereby certified that the annexed document is a true copy of the above-mentioned application, as originally filed on 2000.12.05*

2001.10.09

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PATENTSTYRET
Styret for det industrielle rettsvern

BL. 130 - 5.000 - 02.00 - Hegro Grafisk AS

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5. desember 2000

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Tittel:
Fremgangsmåte og arrangement for synkronisering av en TDM buss.

Fullmektig:
Oslo Patentkontor AS, Postboks 7007 M, N-0306 Oslo

# ARRANGEMENT AND METHOD FOR TRANSMITTING DATA OVER A TDM BUS

## TECHNICAL FIELD

The invention is applicable in the data- and telecommunication field. In particular this invention describes an improved synchronisation and clocking solution related to data communication over a TDM backplane bus.

## TECHNICAL BACKGROUND

A traditional TDM-bus application consists of a data bus (DATA) (usually 8 bits), a data clock (CLK) and a frame synchronisation signal (FS). The time domain is divided into frames where each frame has a fixed duration (usually 125 µs). A frame synchronisation signal indicates the start of each frame and has a period as long as the frame duration. The frame synchronisation signal and the data clock comes from a synchronisation master source and are the timing master signals for all transmitters and receivers that are communicating via the TDM-bus. The frames are divided into a fixed number (N) of timeslots (TS) identified by local timeslot counters (CNT). The local timeslot counters are reset by the FS signal. In each TS data may be transmitted from a transmitter to a receiver using time division multiplexing (TDM).

The synchronisation Master regenerates the frame synchronisation signal from an incoming data stream containing a synchronisation pattern. The data clock is phase locked to the frame synchronisation signal to avoid bit glips during the transmission.

In most TDM-bus applications it is possible to configure more than one synchronisation source and more than one synchronisation master. If the active synchronisation source or the active synchronisation master fails, another will take over according to a priority list. If this happens it is important that the switch over from one data clock to another is done in a controlled way so that no bit faults appear. This is usually solved by phase locking all the synchronisation masters to the active synchronisation master, and at switch over, gradually phase lock the new synchronisation master data clock to the active synchronisation source.

The "H.110 Hardware Compatibility Specification: CT Bus" standard is an example of such a TDM-bus solution as described above.

The problems encountered with this conventional solution are:

1. In a system with a large number of TS within a frame, the data speed increases and the phase locking of the data clock becomes more complicated. Jitter, stability and delay problems introduced in the phase locked loop (PLL) limits the maximum data rate.

2. A controlled switch over from one data clock to another (i.e. if a synchronisation master fails), requires a slow PLL (low bandwidth loop filter) because the data clock must gradually switch over from one synchronisation source to another to avoid bit glips.

3. A slow PLL is complicated to implement in hardware (especially in integrated circuits), and jitter, stability and delay problems become greater the slower the PLL is.

## OTHER PRIOR ART

In US-patent 5,544,324 is disclosed a data communication system, such as local area network, provided with the capability of transmitting isochronous data. Each node includes a free running clock that determines the length of the frames and timeslots. Ideally the clock's frequency is equal to the network frequency. In reality it can be greater or less than the network frequency. This results in a local frame length that departs from the frame length in the signals on the network. To compensate for the variations between local and network frame lengths, timeslots are added or subtracted in some of the frames.

## BRIEF DESCRIPTION OF THE INVENTION

The object of the present invention is to provide an arrangement and method for transmitting data over a TDM bus that allows a faster data transfer while maintaining a controlled switch over from one synchronisation master to another in case the current master should fail.

This object is achieved in an arrangement and method according to the present invention, in which the use of a phase locked data clock is avoided. Said clock is replaced with a free-running clock running at an over frequency in relation to the frame length. However, the exact scope of the invention is as defined in the appended patent claims.

## DETAILED DESCRIPTION OF THE INVENTION

The invention will now be described in detail in reference to the appended drawings, in which:

Fig. 1 shows a simplified block diagram of a TDM bus arrangement according to prior art.

Fig. 2 shows a timing diagram for the TDM bus arrangement in Fig. 1.

Fig. 3 shows a block diagram of a TDM bus arrangement according to the present invention, including a free running data clock.

Fig. 4 shows a timing diagram for the various signals in the inventive TDM bus arrangement shown in Fig. 3.

In Fig. 1 is shown a prior art communication system, with an internal TDM back-plane bus. The system exchanges data with an outside high bit-rate network, typically a PDH network. The PDH network is merely an example on a possible external connection; other network standards may be just as usable, and the type of external network has no influence on the present invention. However, a description of the PDH network can be found in [3].

The application includes transmitters and receivers communicating with the external network, typically with buffers separating the TDM bus from the PDH network serial interfaces.

The internal communication takes place on a TDM bus with a Synchronisation Master supplying the Frame Synchronisation signals and a clock oscillator phase locked to these FS signals, as explained earlier. The SM develops the FS signals from the PDH network in order to get the application synchronised with the incoming signals.

Fig. 2 visualises the timing between the various signals. The FS signal is synchronised to the outside data stream, and the clock signal is in sync with the FS signal due to the PLL. Transmitters and receivers include timeslot counters allowing them to send/receive in the correct timeslot. In the figure CNT indicates the identification (numbering) of the individual timeslots.

However, as mentioned above (item 1 and 3), this solution has its drawbacks, and it is desirable to eliminate the PLL in the synchronisation master block in figure 1.

We will now turn to Fig. 3 that shows a TDM bus system constructed according to the present invention. Instead of the PLL a free-running data clock coming from a stable oscillator independent of the frame synchronisation signal is introduced. In a traditional TDM system this will lead to bit faults because the number of clock periods within a frame will not be exactly fixed from frame to frame, but by doing some modifications, the bit faults can be eliminated:

1. Select the frequency of the data clock oscillator so that the number of periods within a frame is always at least one more than the number of timeslots required. (This results in a dummy time period with no data content within each frame.)

2. The timeslot counter identifying each timeslot must be modified to also identify the dummy time period. This may be done by introducing a carry bit, which is set each time the counter exceeds N (the number of timeslots on the TDM bus).

3. The timeslot counter must be reset by the frame synchronisation signal so that the first timeslot comes on a known time right after the frame synchronisation signal, and so that the dummy time period is at the end of the frame after all the timeslots have been transmitted.

4. The frame synchronisation signal must be synchronised (FS_S) to the free-running independent data clock to obtain synchronism between the involved signals.

5. The problem mentioned above, getting a controlled switch over from one data clock to another, is solved by always performing switch over from one synchronisation master to another during the dummy time period. During this period there is no data transmission so no bit glips will occur.

In this system, the local free running oscillator may not be coincident with the signals on the external network, but the two signals may vary in phase, as indicated on Fig. 4 (the oscillator is lagging by 45°). However, this is a minor problem that is easily solved, e.g. by introducing a delay in the buffers.

ADVANTAGES

The advantages of the proposed solution are:

1. Jitter-, stability- and delay problems introduced in the PLL in figure 1 are eliminated by replacing the PLL with a stable free running oscillator as indicated in figure 3.

2. Synchronisation switchover conditions are simplified.

3. Complicated PLL design is eliminated

4. No variance detection between reference and local clock as described in [2] (column 9) is needed.

5. No frame length adjustment as described in [2] (column 9) is needed.

BROADENING

The invention might be used as a modification of the H.110 standard [1].

REFERENCES

[1] ECTF; Hardware Compatibility Specification: CT Bus

[2] US patent 5,544,324; "Network for transmitting isochronous source data using a frame structure with variable number of time slots to compensate for timing variance between reference clock and data rate."

[3] ITU-T recommendation G.705 (10/00) - Characteristics of Plesiochronous Digital Hierarchy (PDH) equipment functional blocks.

## PATENT CLAIMS

1. Arrangement in a communication system including a TDM bus, a number of transmitters and receivers connected to said bus, at least one synchronisation master developing frame synchronisation signals, a clock oscillator, and a timeslot counter in each transmitter/receiver, c h a r a c t e r i s e d i n that:
- said clock generator is a stable free-running clock generator,
- the frequency of said clock generator is selected to give a number of periods within a frame that is always at least one more than the number of timeslots required, the period(s) exceeding this number constituting a dummy period,
- each timeslot counter is adapted to identify the dummy period,
- the frame synchronisation signals are synchronised to the free-running clock.

2. Arrangement as claimed in claim 1, c h a r a c t e r i s e d i n that the dummy period is identified by introducing a carry bit which is set each time the counter(s) exceeds said number.

3. Arrangement as claimed in claim 2, in a system including several synchronisation masters, c h a r a c t e r i s e d i n that if the active synchronisation master fail, a switch over to another synchronisation master takes place during the dummy period.

4. Method for synchronising a Frame Synchronisation signal (FS) and a data clock signal (CLK) in a TDM-bus system, said system including a number of transmitters and receivers connected to said bus, at least one synchronisation master developing the frame synchronisation signal, a clock oscillator supplying the data clock signal, and a timeslot counter in each transmitter/receiver, c h a r a c t e r i s e d i n that the method includes the following steps:

- to develop the FS signal from an external communication signal,
- to produce the CLK signal from a free running clock oscillator independent of the FS signal,
- to select the frequency of said clock signal (CLK) so that the number of periods within a frame is always at least one more than the number of timeslots required, said period(s) exceeding this number constituting a dummy period,
- to synchronise the FS signal to the CLK signal, and supply this synchronised Frame Synchronising signal (FS-S) to the TDM-bus.

5. Method as claimed in claim 4, c h a r a c t e r i s e d i n that a carry bit is introduced in said timeslot counters to identify said dummy period, said carry bit being set each time the counter(s) exceeds the required number of timeslots on the TDM bus.

6. Method as claimed in claim 5, c h a r a c t e r i s e d i n that if a synchronisation master fail, the system will switch over to another synchronisation master during said dummy period.

**ABSTRACT**

The invention relates to a TDM backplane bus system, in which a Frame Synchronisation signal is developed from an external communication signal, a data clock signal is produced from a free running clock oscillator independent of the FS signal, to select the frequency of said clock signal so that the number of periods within a frame is always at least one more than the number of timeslots required, to synchronise the FS signal to the CLK signal, and supply this synchronised Frame Synchronising signal (FS-S) to the TDM-bus. Further, said exceeding period(s) is identified by introducing a carry bit in the timeslot counters, said carry bit being set each time the counter(s) exceeds the number of timeslots on the TDM bus.

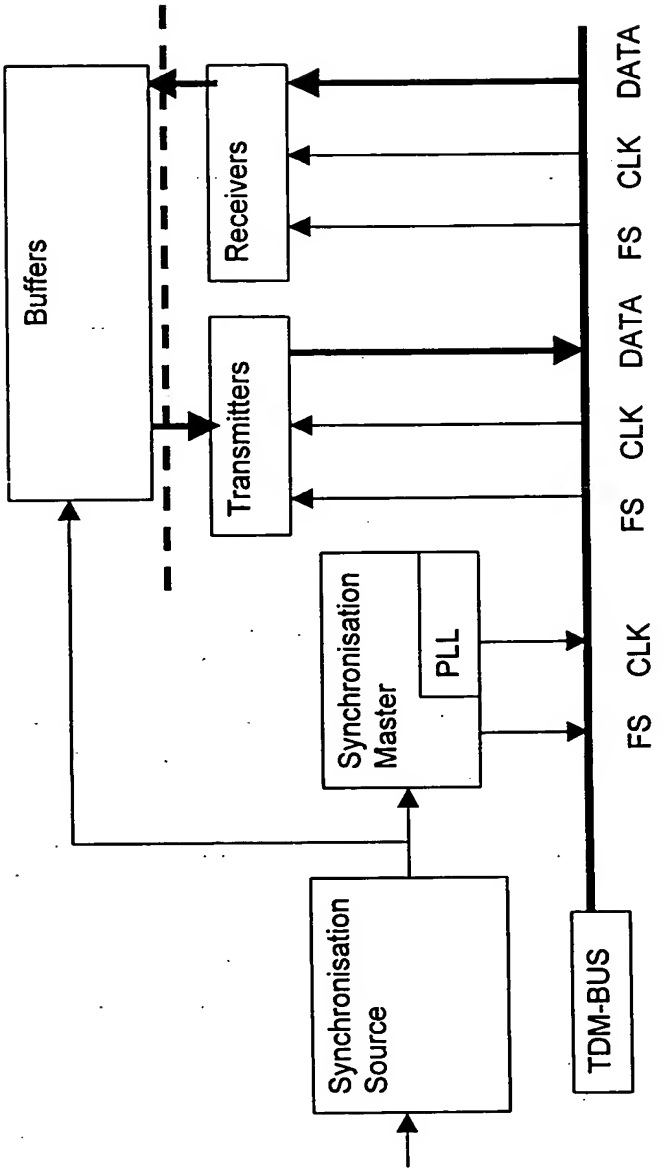


Figure 1

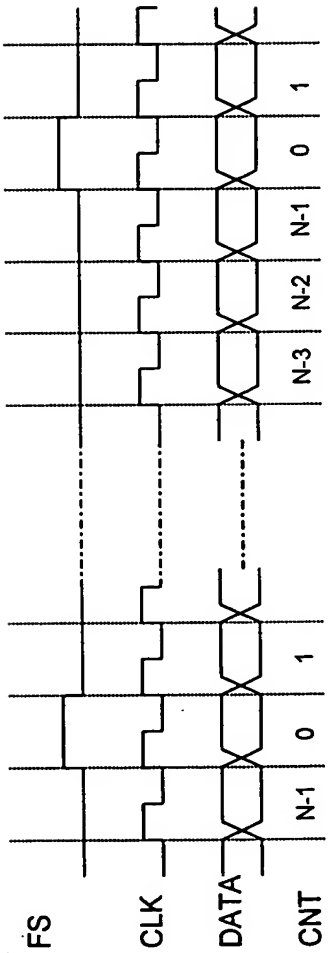


Figure 2

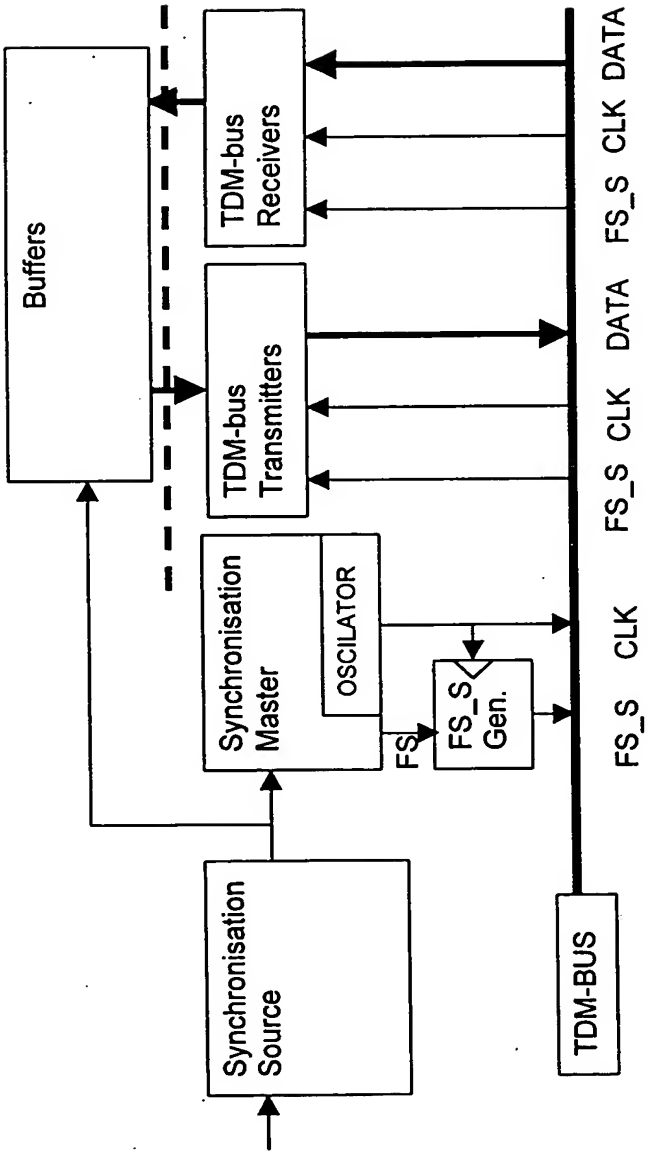
Buffers
TDM-bus Receivers
TDM-bus Transmitters
Synchronisation Master
OSCILATOR
FS
FS_S Gen.
Synchronisation Source
TDM-BUS
FS_S CLK
FS_S CLK DATA
FS_S CLK DATA

Figure 3

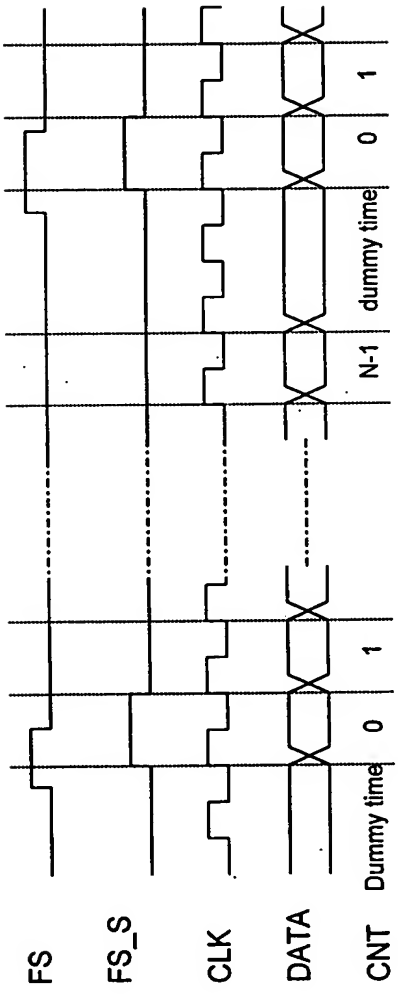


Figure 4